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EXAMINER	
ODOM, CURTIS B	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/598,870	FARLOW, CHARLES S.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/2/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-17,19-26,28-32,35-41 and 43-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19,20 and 52-56* is/are allowed.

6)☒ Claim(s) *1-6,9-17,21-26,28-32,35-41 and 43-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/2/2006 have been fully considered but they are not persuasive. Applicant states there is no motivation to combine Ueda (U. S. Patent No. 5, 787, 118) an Coonce et al. (U. S. Patent No. 4, 064, 370). However, Ueda discloses storing an output or an equalizer in a memory (see Fig. 1, blocks 43 and 44) for an amount of time before the outputs are provided to a selector. Ueda simply does not disclose this amount of time is a time slot of a communication channel. Coonce et al. discloses a plurality of buffer (memory) circuits (Fig. 1, block 205, column 3, line 62-column 4, line 24) which store intermediate signals (column 6, lines 45-54 and column 9, lines 15-19) for the duration of a time slot (976 nanoseconds). Coonce et al. discloses that synchronism throughout the device can be controlled by controlling the timing of the buffer memories using a time slot counter (column 8, lines 8-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory of Ueda with the memory of Coonce et al. in order to process each data path in sequence (Coonce et al., column 4, lines 62-64) and maintain synchronization between the data paths (column 8, lines 8-22). Thus, it is the understanding of the examiner that there is motivation to combine these references.

Applicant states there no motivation to combine the references of Zak (U. S. Patent No. 6, 084, 926) and Yaguchi (U. S. Patent No. 6, 980, 584). However, Yaguchi discloses decoders (see Fig. 4, blocks 413 and 414, column 4, lines 57-63 and column 5, lines 12-16) to decode

signals. Zak futher discloses decoders used to decode signals using forward error correction (see column 4, lines 28-41). Thus, since both references disclose decoders for decoding signals, it would have been obvious to modify the decoders of Yaguchi with the forward error correction decoding of Zak et al. since Zak et al. states forward error correction decoding provide error correction on received data (see column 5, lines 2-11).

Applicant further states there is motivation to combine Yaguchi (U. S. Patent No. 6, 980, 584) and Ueda (U. S. Patent 5, 787, 118). However, Yaguchi discloses an equalizer bank coupled to the input including a first and second channel estimation device and first and second multipliers (Fig. 4, blocks 401, 402, 408, and 409) coupled in parallel, which equalizes incoming signals by performing delay compensation of the incoming signals (column 2, lines 20-23) by multiplying (Fig. 4, blocks 402 and 409) the incoming signals by the complex conjugate of the channel estimation (column 4, lines 49-51). Yaguchi simply does not discloses the equalizers comprises an adaptive linear or non-linear adaptive equalizer with a transversal structure which uses a recursive least squares adaptation algorithm. However, Ueda, discloses selecting between two equalizer outputs (Fig. 1) based on an equalization error (column 20, lines 1-16), wherein the equalizers comprise an adaptive linear (Fig. 1, block 42) equalizer and a decision feedback non-linear adaptive equalizer (Fig. 1, block 41) with a transversal structure (column 9, lines 9-17) which use a recursive least squares (RLS) adaptation algorithm (column 3, lines 26-27) to update coefficients. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yaguchi with the equalizers of Ueda for selection of the best path based on the adaptive equalizers and the decoders since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16). Thus, it is the understanding

of the examiner, there is motivation (reducing performance degradation) to combine the references. Yaguchi also discloses a first decoder bank (Fig. 4, blocks 406, 407, 413, and 414) having at least two frame (packet) decoder circuits (Fig. 4, blocks 413 and 414, column 4, lines 57-63 and column 5, lines 12-16) coupled in parallel, responsive to the equalizer bank. Yaguchi simply does not disclose the decoder bank provides a feedback signal to the equalizers. However, Ueda discloses (Fig. 15) after decoding a signal using a decision circuit (Fig. 15, block 4, column 1, lines 51-56) output from adaptive equalizer filters (Fig. 1, blocks 1 and 2, column 1, lines 40—51), providing a feedback signal though a tap coefficient update (Fig. 1, block 6, column 1, liens 57-59) to the filters. The signal is used to update the taps of the filters of the equalizer, thus, making the equalizer adaptive. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yaguchi to provide a feedback signal to the equalizers as disclosed by Ueda to update the coefficients of the equalizers since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16). Thus, it is the understanding of the examiner, there is motivation (reducing performance degradation) to combine the references.

Applicant further states there is motivation to combine Yaguchi (U. S. Patent No. 6, 980, 584) and Kameya (U. S. Patent No. 4, 313, 202). However, Yaguchi discloses an equalizer bank coupled to the input including a first and second channel estimation device and first and second multipliers (Fig. 4, blocks 401, 402, 408, and 409) coupled in parallel, which equalizes incoming signals by performing delay compensation of the incoming signals (column 2, lines 20-23) by multiplying (Fig. 4, blocks 402 and 409) the incoming signals by the complex conjugate (coefficient) of the channel estimation (column 4, lines 49-51). Kameya further discloses a

filtering method which involves multiplying received signal samples by filter coefficients corresponding to the time slot of the received signal (column 4, lines 36-43). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the equalizers of Yaguchi with the filtering as taught by Kameya to select of the best path based on the filters and the decoders since Kamaya states the filtering can perform compromise equalization (column 5, lines 2-9, wherein equalization compensates for delay). Thus, it is the understanding of the examiner, there is motivation (performing compromise equalization) to combine the references.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 28-32, 35-39, 43, 44, and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (previously cited in Office Action 5/12/2005) in view of Coonce et al. (previously cited in Office Action 1/29/2005).

Regarding claim 1, Ueda discloses an equalization circuit (Fig. 1), comprising:

an input (Fig. 1, block 40) adapted to receive signals from a communications channel;

a plurality of equalizer circuits (Fig. 1, blocks 41 and 42) coupled to the input and operable to generate a plurality of intermediate signals;

a selector circuit (Fig. 1, block 48) responsive to the equalizer circuits that selects one of the intermediate signals; and

an output (Fig. 1, output of block 48) coupled to the selector circuit that receives the selected intermediate signal.

Ueda does not disclose a plurality of buffer circuits, each buffer circuit coupled between one of the plurality of equalizer circuits and the selector circuit to buffer the intermediate signals for approximately the duration of a time slot of the communication channel.

Coonce et al. discloses a plurality of buffer circuits (Fig. 1, block 205, column 3, line 62- column 4, line 24) which buffer intermediate signals (column 6, lines 45-54 and column 9, lines 15-19) for the duration of a time slot (976 nanoseconds). Coonce et al. discloses that synchronism throughout the device can be controlled by controlling the timing of the buffer memories using a time slot counter (column 8, lines 8-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the equalizer of Ueda with the teachings of Coonce et al. in order to process each data path in sequence (Coonce et al., column 4, lines 62-64) and maintain synchronization between the data paths (column 8, lines 8-22).

Regarding claim 2, which inherits the limitations of claim 1, Ueda et al. discloses the equalizer circuits comprise adaptive equalizers (column 19, line 65- column 20, line 10).

Regarding claim 3, which inherits the limitations of claim 2, Ueda et al. discloses the adaptive equalizers comprise a linear adaptive equalizer an non-linear decision feedback equalizers (column 19, line 65-column 20, line 11).

Regarding claim 4, which inherits the limitations of claim 2, Ueda discloses each of the adaptive equalizers comprises a transversal structure (column 9, lines 9-15).

Regarding claim 5, which inherits the limitations of claim 2, Ueda discloses each of the adaptive equalizers uses a least mean square error algorithm (column 25, lines 41-45).

Regarding claim 6, which inherits the limitations of claim 1, Ueda discloses the equalizer circuits provides a signals that reflects the relative quality (error values) of the intermediate signals from a plurality of equalizer circuits to the selector circuit to select the intermediate signal (column 20, line 61-column 21, line 17).

Regarding claims 28, Ueda and Coonce et al. discloses all the limitations of claim 28 (see rejection of claim 1) including an antenna for receiving a signal over a communication channel (see Ueda, Fig. 11, element 101).

Regarding claim 29, Ueda further discloses an antenna for receiving a signal over a wireless communication channel (Fig. 11, element 101).

Regarding claim 30, Uedu and Coonce et al. do not disclose receiving the signal over a communication channel of a hybrid fiber coax network. However, Ueda does disclose performing equalization of any time-varying channel (column 8, lines 13-18). Therefore, it would have been obvious to one skilled in the art at the time the invention was made that Ueda and Coonce et al.could have applied equalization to a time-varying communication channel of a hybrid fiber coax network.

Regarding claim 31, Ueda further discloses equalizing the signal in a bank of equalizers (Fig. 1, blocks 41 and 42).

Regarding claim 32, Ueda further discloses loading selected tap coefficients for a plurality of equalizers during a training mode prior to receiving a signal over the communication channel (Ueda, column 3, line 5-column 4, line 22).

Regarding claim 35, Ueda further discloses generating a quality measure of the output of the equalizers (column 20, lines 61-67).

Regarding claim 36, Ueda further discloses the quality measure is a mean (integrated) square error (column 20, lines 61-67).

Regarding claim 37, Ueda discloses a method for equalizing a signal from a time division multiple access communication channel, the method comprising:

receiving (Fig 11, block 101) a signal over the communication channel using an antennal;

equalizing (Fig. 1, blocks 41 and 42) the signal in parallel in a bank of adaptive equalizers with parallel outputs (column 19, line 65-column 20, line 10);

further (Fig. 1, blocks 43 and 44) processing the parallel outputs of the bank of adaptive equalizers using a memory;

generating (column 20, lines 61-67) a quality measure (integrated square error) of the output of each of the bank of adaptive equalizers; and

selecting (column 21, lines 7-17) an output of one of the equalizers based on the quality measure using a comparator and a selector switch.

Ueda does not buffering the outputs of the equalizers for approximately the duration of a time slot of the communication channel.

Coonce et al. discloses a plurality of buffer circuits (Fig. 1, block 205, column 3, line 62-column 4, line 24) which buffer intermediate signals (column 6, lines 45-54 and column 9, lines 15-19) for the duration of a time slot (976 nanoseconds). Coonce et al. discloses that synchronism throughout the device can be controlled by controlling the timing of the buffer memories using a time slot counter (column 8, lines 8-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the equalizer of Ueda with the teachings of Coonce et al. in order to process each data path in sequence (Coonce et al., column 4, lines 62-64) and maintain synchronization between the data paths (column 8, lines 8-22).

Regarding claim 38, the claim includes limitations similar to the above rejection of claim 29, which is applicable hereto.

Regarding claim 39, claim includes limitations similar to the above rejection of claim 30, which is applicable hereto.

Regarding claim 43, claim includes limitations similar to the above rejection of claim 1, which is applicable hereto.

Regarding claim 44, claim includes limitations similar to the above rejection of claim 2, which is applicable hereto.

Regarding claim 49, Ueda discloses a telecommunications systems, comprising:

at least one transmission system (Ueda, column 1, lines 10-16) representing a base station which can provide connection to a core network including a circuit that receives signals (Ueda,

Fig. 1 and Fig. 11) from the core network and provides the signal to a plurality of mobile communication users (Ueda, column 1, lines 10-16) over at least one communication channel, wherein the transmission system includes an equalization circuit (Fig. 1 and Fig. 11), comprising:

a plurality of equalizer circuits (Fig. 1, blocks 41 and 42) coupled to the input and operable to generate a plurality of intermediate signals;

a selector circuit (Fig. 1, block 48) responsive to the equalizer circuits that selects one of the intermediate signals; and

an output (Fig. 1, output of block 48) coupled to the selector circuit that receives the selected intermediate signal.

Ueda does not disclose a plurality of buffer circuits, each buffer circuit coupled between one of the plurality of equalizer circuits and the selector circuit to buffer the intermediate signals for approximately the duration of a time slot of the communication channel which would allow the transmission system to receive time division multiple access signals.

Coonce et al. discloses a plurality of buffer circuits (Fig. 1, block 205, column 3, line 62-column 4, line 24) which buffer intermediate signals (column 6, lines 45-54 and column 9, lines 15-19) for the duration of a time slot (976 nanoseconds). Coonce et al. discloses that synchronism throughout the device can be controlled by controlling the timing of the buffer memories using a time slot counter (column 8, lines 8-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the equalizer of Ueda with the teachings of Coonce et al. in order to process each data path in sequence (Coonce et al., column 4, lines 62-64) and maintain synchronization between the data

paths (column 8, lines 8-22). The addition of the buffers would allow the transmission system of Ueda to receive time division multiple access signals.

Regarding claim 50, Ueda discloses the transmission system comprises a wireless transmission system (Fig. 11).

Regarding claim 51, Uedu and Coonce et al. do not disclose the transmission system comprises a head end of a hybrid fiber coax network. However, Ueda does disclose performing equalization of any time-varying channel (column 8, lines 13-18). Therefore, it would have been obvious to one skilled in the art at the time the invention was made that Ueda and Coonce et al.could have applied equalization in the transmission system to a time-varying communication channel of a hybrid fiber coax network. Thus, the transmission system could have been a head-end of a hybrid fiber coax network.

4. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yaguchi (previously cited in Office Action 5/31/2006) in view of Zak et al. (previously cited in Office Action 5/31/2006).

Regarding claim 9, Yaguchi discloses an equalization circuit (Fig. 4) comprising:

a matched filter input (Fig. 4, reception signal) adapted to receive signals from a communication channel;

an equalizer bank coupled to the input including a first and second channel estimation device and first and second multipliers (Fig. 4, blocks 401, 402, 408, and 409) coupled in parallel, which equalizes incoming signals by performing delay compensation of the incoming signals (column 2, lines 20-23) by multiplying (Fig: 4, blocks 402 and 409) the incoming signals by the complex conjugate of the channel estimation (column 4, lines 49-51);

a first decoder bank (Fig. 4, blocks 406, 407, 413, and 414) having at least two frame (packet) decoder circuits (Fig. 4, blocks 413 and 414, column 4, lines 57-63 and column 5, lines 12-16) coupled in parallel, responsive to the equalizer bank;

a selector circuit (Fig. 4, block 415, column 5, lines 17-22) coupled to the decoder bank that selects an output signal of one of the at least two equalizer (delay compensation) circuits based on processing of a CRC for frame loss in the decoder bank; and

an output (output of block 415) coupled to the selector circuit that receives the selected demodulated output signal.

Yaguchi does not disclose the frame decoder circuits are error correction decoder circuits.

However, Zak et al. discloses selecting the output of a data path (Fig. 1), one of which includes an equalizer (Fig. 1, block 26) based on the outputs of two decoders which include forward error correction (column 4, lines 28-41).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the decoders of Yaguchi with forward error correction (FEC) as taught by Zak et al. since Zak et al. states FEC can provide error corrections on the received data (column 5, lines 2-11).

Regarding claim 10, Zak et al. further discloses the decoders use forward error correction (column 4, lines 28-41). It would have been obvious to include this feature since Zak et al. states FEC can provide error corrections on the received data (column 5, lines 2-11).

5. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yaguchi (previously cited in Office Action 5/31/2006) in view of Ueda (previously cited in Office Action 5/12/2005).

Regarding claims 21-24, Yaguchi discloses an equalization circuit comprising:

a matched filter input (Fig. 4, reception signal) adapted to receive signals from a communication channel;

an equalizer bank including fixed equalizers coupled to the input including a first and second channel estimation device and first and second multipliers (Fig. 4, blocks 401, 402, 408, and 409) coupled in parallel, which equalizes incoming signals by performing delay compensation of the incoming signals (column 2, lines 20-23) by multiplying (Fig. 4, blocks 402 and 409) the incoming signals by the complex conjugate of the channel estimation (column 4, lines 49-51);

a first decoder bank (Fig. 4, blocks 406, 407, 413, and 414) having at least two frame (packet) decoder circuits (Fig. 4, blocks 413 and 414, column 4, lines 57-63 and column 5, lines 12-16) coupled in parallel, responsive to the equalizer bank;

a selector circuit (Fig. 4, block 415, olumn 5, lines 17-22) coupled to the decoder bank that selects an output signal of one of the at least two equalizer (delay compensation) circuits based on processing of a CRC for frame loss in the decoder bank; and

an output (output of block 415) coupled to the selector circuit that receives the selected demodulated output signal.

Yaguchi does not disclose the equalizers comprise an adaptive linear or non-linear adaptive equalizer with a transversal structure which uses a recursive least squares adaptation algorithm.

However, Ueda, discloses selecting between two equalizer outputs (Fig. 1) based on an equalization error (column 20, lines 1-16), wherein the equalizers comprise an adaptive linear

(Fig. 1, block 42) equalizer and a decision feedback non-linear adaptive equalizer (Fig. 1, block 41) with a transversal structure (column 9, lines 9-17) which use a recursive least squares (RLS) adaptation algorithm (column 3, lines 26-27) to update coefficients. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yaguchi with the equalizers of Ueda for selection of the best path based on the adaptive equalizers and the decoders since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16).

Regarding claim 25, Yaguchi discloses an equalizer circuit comprising

a matched filter input (Fig. 4, reception signal) adapted to receive signals from a communication channel;

an equalizer bank coupled to the input including a first and second channel estimation device and first and second multipliers (Fig. 4, blocks 401, 402, 408, and 409) coupled in parallel, which equalizes incoming signals by performing delay compensation of the incoming signals (column 2, lines 20-23) by multiplying (Fig. 4, blocks 402 and 409) the incoming signals by the complex conjugate of the channel estimation (column 4, lines 49-51);

a first decoder bank (Fig. 4, blocks 406, 407, 413, and 414) having at least two frame (packet) decoder circuits (Fig. 4, blocks 413 and 414, column 4, lines 57-63 and column 5, lines 12-16) coupled in parallel, responsive to the equalizer bank;

a selector circuit (Fig. 4, block 415, olumn 5, lines 17-22) coupled to the decoder bank that selects an output signal of one of the at least two equalizer (delay compensation) circuits based on processing of a CRC for frame loss in the decoder bank; and

an output (output of block 415) coupled to the selector circuit that receives the selected demodulated output signal.

Yaguchi does not disclose the decoder bank provides a feedback signal to the equalizers.

However, Ueda discloses (Fig. 15) after decoding a signal using a decision circuit (Fig. 15, block 4, column 1, lines 51-56) output from adaptive equalizer filters (Fig. 1, blocks 1 and 2, column 1, lines 40—51), providing a feedback signal though a tap coefficient update (Fig. 1, block 6, column 1, liens 57-59) to the filters. The signal is used to update the taps of the filters of the equalizer, thus, making the equalizer adaptive. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yaguchi to provide a feedback signal to the equalizers as disclosed by Ueda to update the coefficients of the equalizers since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16).

Regarding claim 26, Ueda further discloses the feedback error (difference) signal is also provided to a selector (comparator) circuit (column 20, lines 49-67) to be used in selecting the output of one of at least two equalizer circuits (column 21, lines 7-17). It would have been obvious to include this feature since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16).

6. Claims 45 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yaguchi (previously cited in Office Action 5/31/2006) in view Kameya (previously cited in Office Action 5/31/2006).

Regarding claim 45, Yaguchi discloses all the limitations of claim 45 (see rejection of claim 18) except the equalization method involves loading coefficients for a selected for a time slot of the communications channel.

However, Kameya discloses a filtering method which involves multiplying received signal samples by filter coefficients corresponding to the time slot of the received signal (column 4, lines 36-43). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the equalizers of Yaguchi with the filtering as taught by Kameya to select of the best path based on the filters and the decoders since Kamaya states the filtering can perform compromise equalization (column 5, lines 2-9, wherein equalization compensates for delay).

Regarding claim 48, Yaguchi further discloses checking for errors at the frame (packet) level (column 5, lines 11-16).

7 Claims 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yaguchi (previously cited in Office Action 5/31/2006) in view of Zak et al. (previously cited in Office Action 5/31/2006) and applied to claim 9, and in further view of Ueda (previously cited in Office Action 5/12/2005).

Regarding claims 11-14, Yaguchi and Zak et al. do not disclose the equalizers comprise an adaptive linear or non-linear adaptive equalizer with a transversal structure which uses a recursive least squares adaptation algorithm.

However, Ueda, discloses selecting between two equalizer outputs (Fig. 1) based on an equalization error (column 20, lines 1-16), wherein the equalizers comprise an adaptive linear (Fig. 1, block 42) equalizer and a decision feedback non-linear adaptive equalizer (Fig. 1, block

41) with a transversal structure (column 9, lines 9-17) which use a recursive least squares (RLS) adaptation algorithm (column 3, lines 26-27) to update coefficients. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yaguchi and Zak etal. with the equalizers of Ueda for selection of the best path based on the adaptive equalizers and the decoders since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16).

Regarding claim 15, Yaguchi and Zak et al. do not disclose the decoder bank provides a feedback signal to the equalizers.

However, Ueda discloses (Fig. 15) after decoding a signal using a decision circuit (Fig. 15, block 4, column 1, lines 51-56) output from adaptive equalizer filters (Fig. 1, blocks 1 and 2, column 1, lines 40—51), providing a feedback signal though a tap coefficient update (Fig. 1, block 6, column 1, liens 57-59) to the filters. The signal is used to update the taps of the filters of the equalizer, thus, making the equalizer adaptive. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yaguchi and Zak et al. to provide a feedback signal to the equalizers as disclosed by Ueda to update the coefficients of the equalizers since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16).

Regarding claim 16, Ueda further discloses the feedback error (difference) signal is also provided to a selector (comparator) circuit (column 20, lines 49-67) to be used in selecting the output of one of at least two equalizer circuits (column 21, lines 7-17). It would have been obvious to include this feature since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yaguchi (previously cited in Office Action 5/31/2006) in view of Zak et al. (previously cited in Office Action 5/31/2006) and applied to claim 9, and in further view of Coonce et al. (previously cited in Office Action 1/29/2005).

Regarding claim 17, Yaguchi and Zak et al. do not disclose the decoder bank includes a buffer circuit.

However, Coonce et al. discloses a plurality of buffer circuits (Fig. 1, block 205, column 3, line 62-column 4, line 24) which buffer intermediate signals (column 6, lines 45-54 and column 9, lines 15-19) for the duration of a time slot (976 nanoseconds). Coonce et al. discloses that synchronism throughout the device can be controlled by controlling the timing of the buffer memories using a time slot counter (column 8, lines 8-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Yaguchi and Zak with the teachings of Coonce et al. in order to process each data path in sequence (Coonce et al., column 4, lines 62-64) and maintain synchronization between the data paths (column 8, lines 8-22).

9. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (previously cited in Office Action 5/12/2005) in view of Coonce et al. (previously cited in Office Action 1/29/2005) as applied to claim 37, in further view of Zak et al. (previously cited in Office Action 5/31/2006).

Regarding claims 40 and 41, Ueda and Coonce et al. do not disclose the further processing comprises forward error correcting or detecting errors at the packet level.

However, Zak et al. discloses selecting the output of two data paths (Fig. 1), one of which includes an equalizer (Fig. 1, block 26) based on the outputs of two decoders which include forward error correction (column 4, lines 28-41) and detecting error of frame (packets) using CRCs (column 4, lines 42-53). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the processing of Ueda and Coonce et al. with forward error correction (FEC) and CRCs as taught by Zak et al. since Zak et al. states FEC and CRCs can provide error detection and corrections on the received data (column 4, lines 41-53 and column 5, lines 2-11).

10. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yaguchi (previously cited in Office Action 5/31/2006) in view Kameya (previously cited in Office Action 5/31/2006) as applied to claim 45, and in further view of Ueda (previously cited in Office Action 5/12/2005).

Regarding claim 46, Yaguchi and Kameya do not disclose equalizing the signal with a plurality of adaptive equalizers.

However, Ueda, discloses selecting between two adaptive equalizer outputs (Fig. 1) based on an equalization error (column 20, lines 1-16), wherein the equalizers comprise an adaptive linear (Fig. 1, block 42) equalizer and a decision feedback non-linear adaptive equalizer (Fig. 1, block 41) with a transversal structure (column 9, lines 9-17) which use a recursive least squares (RLS) adaptation algorithm (column 3, lines 26-27) to update coefficients. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device of Yaguchi and Kameya with the equalizers of Ueda for selection of the best path

based on the adaptive equalizers and the decoders since Ueda states adaptive equalizers reduce performance degradation (column 1, lines 10-16).

11. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yaguchi (previously cited in Office Action 5/31/2006) in view Kameya (previously cited in Office Action 5/31/2006) as applied to claim 45, and in further view of Zak et al. (U. S. Patent No. 6, 084, 926).

Regarding claims 47, Yaguchi and Kameya do not disclose the further processing comprises forward error correcting the equalized signals.

However, Zak et al. discloses selecting the output of two data paths (Fig. 1), one of which includes an equalizer (Fig. 1, block 26) based on the outputs of two decoders which include forward error correction (column 4, lines 28-41) and detecting error of frame (packets) using CRCs (column 4, lines 42-53). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the processing of Yaguchi and Kameya with forward error correction (FEC) and CRCs as taught by Zak et al. since Zak et al. states FEC and CRCs can provide error detection and corrections on the received data (column 4, lines 41-53 and column 5, lines 2-11).

Allowable Subject Matter

10. Claims 19, 20, and 52-56 are allowable over prior art references because related references do not discloses a first equalizer bank and first and second decoder bank coupled to the equalizer, wherein an output of on of the equalizers is selected.

Conclusion

11. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Curtis Odom
December 10, 2006

JAY K. PATEL
SUPERVISORY PATENT EXAMINER